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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,389	12/10/2003	Takayuki Katoh	JP920020250US1	1388

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EXAMINER
YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,389	KATOH ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-19* is/are rejected.

7)☒ Claim(s) *7, 8 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 2/5/03. It is noted, however, that applicant has not filed a certified copy of the 2003/028377 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voegeli et al., US Patent no. 6,651,178 [Voegeli], in view of Applicant's Admitted Prior Art [AAPA].

Regarding claim 1, Voegeli discloses a power supply controller [Power System Controller in Figure 1] which directs the supply of a plurality of different voltages from a power supply unit, comprising:

a state register circuit to store state values [VID codes] corresponding to a combination of voltages supplied by the power supply unit [inherent that VID codes are stored in some type of register, column 5, lines 35-50 and column 6, lines 19-23];

a reference clock oscillator circuit [inherent that some sort of clock is supplied to power system controller circuit];

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit [power system controller sends voltage level and turn-on sequence information over the power control bus to the plurality of voltage supplying circuits, column 6, lines 57-67]; and

an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by said state value changing combination circuit to the power supply unit [power control bus, column 6, lines 57-67].

Voegeli discloses that the power system controller may specify a turn-on sequence for the plurality of power supplies, but does not disclose changing the state values one by one in a predetermined order corresponding to a target combination of voltages when the change instruction is received to change the combination of voltages supplied by the power supply unit. AAPA discloses changing output voltages sequentially in a predetermined order to prevent destruction or malfunction to circuitry [paragraph 0005]. It would have been obvious to one of ordinary skill in the art to modify the Voegeli controller to change output voltages of the power supplies sequentially in a predetermined order for the motivation of preventing destruction or malfunction to circuitry in the system [AAPA, paragraph 0005].

Regarding claim 2, AAPA further discloses that the change instruction specifying a power on sequence of the combination of supplied voltages starts with the lowest supplied voltage [paragraph 0005].

Regarding claim 3, AAPA further discloses that the change instruction specifying a power off sequence of the combination of supplied voltages, starts from the highest supplied voltage [paragraph 0005].

Regarding claim 4, Voegeli and AAPA, as described above, disclose a state register circuit that has state values of combinations of voltages, changing the state values in a predetermined order indicating for which one voltages should be changed first; and an output section that supplies the combinations of voltages corresponding to the state values changed one by one. AAPA further discloses an information processor to which the plurality of voltages are supplied, which has a plurality of sections operating on the plurality of voltages [paragraph 0004].

Regarding claims 5 and 6, Voegeli and AAPA do not disclose enabling the reference clock when it is needed and disabling the reference clock when it is not needed. However, enabling a clock when it is needed and disabling the clock when it is not needed is a well known way of conserving power in a computer system. Therefore, it would have been obvious to one of ordinary skill in the art to enable the reference clock, in the Voegeli and AAPA system, when it is needed and disabling the reference clock when it is not needed for the well known advantage of reducing unnecessary power consumption of the system.

Regarding claim 9, Voegeli discloses a power supply controller [Power System Controller in Figure 1] which controls a power supply unit having a plurality of power supplies each of which can be independently set to a plurality of states, said power supply controller comprising:

a state register circuit to store state values [VID codes] corresponding to a combination of voltages supplied by the power supply unit [inherent that VID codes are stored in some type of register, column 5, lines 35-50 and column 6, lines 19-23];

a reference clock oscillator [inherent that some sort of clock is supplied to power system controller circuit];

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit [power system controller sends voltage level and turn-on sequence information over the power control bus to the plurality of voltage supplying circuits, column 6, lines 57-67];

an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by the state value changing combination circuit to the power supply unit [power control bus, column 6, lines 57-67].

Voegeli discloses that the power system controller may specify a turn-on sequence for the plurality of power supplies, but does not disclose changing the state values one by one in a predetermined order corresponding to a target combination of voltages when the change instruction is received to change the combination of voltages supplied by the power supply unit. AAPA discloses changing output voltages sequentially in a predetermined order to prevent destruction or malfunction to circuitry [paragraph 0005]. It would have been obvious to one of ordinary skill in the art to modify the Voegeli controller to change output voltages of the power supplies sequentially in a predetermined order for the motivation of preventing destruction or malfunction to circuitry in the system [AAPA, paragraph 0005].

Regarding claims 10 and 11, Voegeli and AAPA, as described above, disclose a state register circuit that has state values of combinations of voltages, changing the state values in a predetermined order indicating for which one voltages should be changed first; and an output section that supplies the combinations of voltages corresponding to the state values changed one

by one. AAPA further discloses an information processor to which the plurality of voltages are supplied, which has a plurality of sections operating on the plurality of voltages [paragraph 0004].

Regarding claims 12 and 13, Voegeli and AAPA do not disclose enabling the reference clock when it is needed and disabling the reference clock when it is not needed. However, enabling a clock when it is needed and disabling the clock when it is not needed is a well known way of conserving power in a computer system. Therefore, it would have been obvious to one of ordinary skill in the art to enable the reference clock, in the Voegeli and AAPA system, when it is needed and disabling the reference clock when it is not needed for the well known advantage of reducing unnecessary power consumption of the system.

Regarding claim 14, Voegeli and AAPA, as described above, disclose a state register circuit that has state values of combinations of voltages, changing the state values in a predetermined order indicating for which one voltages should be changed first; and an output section that supplies the combinations of voltages corresponding to the state values changed one by one. AAPA further discloses an information processor to which the plurality of voltages are supplied, which has a plurality of sections operating on the plurality of voltages [paragraph 0004].

Regarding claim 15, Voegeli discloses a method of supplying a plurality of voltages from a multiple voltage level power supply to an information processor, the method comprising the steps of:

providing a state register circuit to store state values [VID codes] corresponding to a combination of voltages supplied by the power supply unit [inherent that VID codes are stored in some type of register, column 5, lines 35-50 and column 6, lines 19-23];

providing a reference clock oscillator circuit [inherent that some sort of clock is supplied to power system controller circuit];

providing a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit [power system controller sends voltage level and turn-on sequence information over the power control bus to the plurality of voltage supplying circuits, column 6, lines 57-67]; and

providing an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by said state value changing combination circuit to the power supply unit [power control bus, column 6, lines 57-67].

Voegeli discloses that the power system controller may specify a turn-on sequence for the plurality of power supplies, but does not disclose changing the state values one by one in a predetermined order corresponding to a target combination of voltages when the change instruction is received to change the combination of voltages supplied by the power supply unit. AAPA discloses changing output voltages sequentially in a predetermined order to prevent destruction or malfunction to an information processor [paragraphs 0004 and 0005]. It would have been obvious to one of ordinary skill in the art to modify the Voegeli controller to change output voltages of the power supplies sequentially in a predetermined order for the motivation of preventing destruction or malfunction to circuitry in the system [AAPA, paragraph 0005].

Regarding claim 16, AAPA further discloses that a change instruction specifying a power on sequence of the combination of supplied voltages starts with the lowest supplied voltage and a change instruction specifying a power off sequence of the combination of supplied voltages starts from the highest supplied voltage [paragraph 0005].

Regarding claim 17, Voegeli and AAPA, as described above, disclose a state register circuit that has state values of combinations of voltages, changing the state values in a predetermined order indicating for which one voltages should be changed first; and an output section that supplies the combinations of voltages corresponding to the state values changed one by one. AAPA further discloses an information processor to which the plurality of voltages are supplied, which has a plurality of sections operating on the plurality of voltages [paragraph 0004].

Regarding claims 18 and 19, Voegeli and AAPA do not disclose enabling the reference clock when it is needed and disabling the reference clock when it is not needed. However, enabling a clock when it is needed and disabling the clock when it is not needed is a well known way of conserving power in a computer system. Therefore, it would have been obvious to one of ordinary skill in the art to enable the reference clock, in the Voegeli and AAPA system, when it is needed and disabling the reference clock when it is not needed for the well known advantage of reducing unnecessary power consumption of the system.

Allowable Subject Matter

Claims 7, 8 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Woo, US Patent no. 7,013,402, discloses a circuit for applying power to a mixed mode integrated circuit.

Rowe, US Patent no. 6,917,123 discloses a power-up control circuit for controlling initial application of power to a system with multiple loads.

Orr et al, US Patent no. 6,850,048, discloses a power supply controller for controlling the power up and power down sequences of a power supply.

Ostojic, US Patent no. 6,771,052, discloses a power supply with a plurality of programmable output voltages.

Mott et al., US Patent no. 6,738,915, discloses supplying multiple voltages to devices in a predictable sequence.

Amin et al., US Patent no. 6,333,650, discloses a voltage sequencing circuit for powering-up sensitive electrical components.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
June 25, 2006

James K. Trujillo
PATENT EXAMINER
TC 2100